REMARKS

Claims 1-21 are pending in the application. Claims 17-21 are withdrawn from consideration as being directed to non-elected inventions. In the Final Office Action of November 4, 2002, the Examiner made the following disposition:

A.) Rejected claims 1-4 under 35 U.S.C. §102(e) as being anticipated by *Fjelstad.*

B.) Rejected claims 7-10 under 35 U.S.C. §102(b) as being anticipated by *Eichelberger.*

C.) Rejected claims 13-14 under 35 U.S.C. §102(e) as being anticipated by *Fillion et al.*

D.) Rejected claims 5-6 under 35 U.S.C. §103(a) as being unpatentable over *Fjelstad* in view of *Sharma.*

E.) Rejected claims 15-16 under 35 U.S.C. §103(a) as being unpatentable over *Fillion et al.* in view of *Sharma.*

F.) Rejected claim 11 under 35 U.S.C. §103(a) as being unpatentable over *Eichelberger* in view of *Sharma.*

G.) Rejected claim 12 under 35 U.S.C. §103(a) as being unpatentable over *Eichelberger* in view of *Sharma.*

Applicants respectfully traverse the rejections and addresses the Examiner's disposition below.

A.) Rejection of claims 1-4 under 35 U.S.C. §102(e) as being anticipated by *Fjelstad*:

Applicants respectfully disagree with the rejection.

Applicants' independent claim 1 has been amended to clarify that the insulation film is a single-layer insulation film. Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned **"VERSION WITH MARKING TO SHOW CHANGES MADE**.

Claim 1, as amended, claims a semiconductor device comprising a plurality of semiconductor chips mounted on an outer surface of a substrate. A single-layer insulation film is provided on the substrate, wherein a top surface and side surfaces of the plurality of semiconductor chips are encrusted in the insulation film. Wiring is provided on the insulation film, wherein the wiring is connected to the plurality of semiconductor chips through a connection hole formed on the insulation film.

Thus, Applicants' claimed semiconductor device is easy to manufacture, since its requires formation of a single-layer insulation film, instead of a multi-layered insulation film.

This is clearly unlike *Fjelstad*, which fails to disclose or even suggest a wiring connected to a chip through a connection hole formed in a single-layer insulation film. Referring to *Fjelstad* Figure 15, *Fjelstad* discloses encasing a peripheral portion of a chip 900 in a first compliant layer 940. (Col. 16, lines 7-15). As clearly shown in Figure 15, the central portion of the top surface of the chip 900 is not encased in the first compliant layer 940. The first compliant layer 940 has downward sloping sides toward the top surface of the chip 900. Wiring 970 is then formed on the downward sloping sides of the first compliant layer 940 and connected to the chip 900. (Col. 16, lines 15-16). Then, a second compliant layer 941 is formed to encapsulate the exposed top surface of the chip 900, the downward-sloping portion of the wiring 970, and the exposed downward-sloping portion of the first compliant layer 940. (Col. 16, lines 19-21).

Thus, unlike Applicants' claim 1 that claims a single-layer insulation film having a connection hole for connecting wiring to a chip, *Fjelstad* teaches two compliant layers 940 and 941 sandwiching a wiring 970 with no connection hole. In other words, unlike Applicants claim 1, *Fjelstad* disclose neither a single-layer insulation film nor a connection hole formed in a single-layer insulation film. Instead, *Fjelstad* merely sandwiches its wiring 970 between a first compliant layer 940 and a second compliant layer 941. Since *Fjelstad* forms its second compliant layer 941 after its first compliant layer 940, *Fjelstad* fails to disclose (and teaches away from) forming a connection hole through a single-layer insulation film to a chip.

Therefore, *Fjelstad* fails to disclose or even suggest Applicants' claim 1.

Further, Applicants respectfully note that the Examiner states that element *Fjelstad* element 955 is a connection hole for connecting *Fjelstad's* wiring to its chip (see Figure 15). Applicants respectfully disagree. *Fjelstad* element 955 is merely a portion of the first compliant layer 940 located next to the chip 900. Contrary to the Examiner's assertion, *Fjelstad's* wiring 970 does not connect to the chip 900 via element 955.

Claims 2-4 depend directly or indirectly from claim 1 and are therefore allowable for at least the same reasons that claim 1 is allowable.

B.) Rejection of claims 7-10 under 35 U.S.C. §102(b) as being anticipated by *Eichelberger*:

Applicants respectfully disagree with the rejection.

Similar to Applicants' claim 1, Applicants' independent claim 7 has been amended to clarify that the insulation film is a single-layer insulation film.

Claim 7, as amended, claims a semiconductor device comprising a plurality of semiconductor chips. A single-layer insulation layer supports the plurality of semiconductor chips, wherein a top surface and at least a portion of side surfaces of the plurality of semiconductor chips are encrusted in the insulation layer and a surface opposite the top surface of the plurality of semiconductor chips is exposed. Wiring is provided on the insulation layer, wherein the wiring is connected to each semiconductor chip of the plurality of semiconductor chips through a connection hole formed on the insulation layer.

Thus, Applicants' claimed semiconductor device is easy to manufacture, since its requires formation of a single-layer insulation film, instead of a multi-layered insulation film.

This is clearly unlike *Eichelberger*, which fails to disclose or even suggest a single-layer insulation layer that encrusts a top surface and at least a portion of side surfaces of a plurality of chips. Referring to *Eichelberger* Figure 5g, *Eichelberger* discloses encasing the sides of a chip 102 in a structure material 104 and then covering the top of the chip with a first dielectric layer 106. As clearly shown in Figure 5g, unlike Applicants' claim 7, *Eichelberger's* chip is not encrusted in a single-layer insulation layer. Instead, the sides of *Eichelberger's* chip are encrusted in the structure material 104, and the top of *Eichelberger's* chip is covered by the first dielectric layer 106. The first dielectric layer 106 does not encrust the sides of *Eichelberger's* chip.

Therefore, *Eichelberger* fails to disclose or even suggest Applicants' claim 7.

Claims 8-10 depend directly or indirectly from claim 7 and are therefore allowable for at least the same reasons that claim 7 is allowable.

Applicants respectfully submit the rejection has been overcome and request that it be withdrawn.

C.) Rejection of claims 13-14 under 35 U.S.C. §102(e) as being anticipated by *Fillion et al.*:

Claims 13-14 have been cancelled.

Applicants respectfully submit that the rejection has been overcome and request that it be withdrawn.

D.) Rejection of claims 5-6 under 35 U.S.C. §103(a) as being unpatentable over *Fjelstad* in view of *Sharma*:

Applicants respectfully disagree with the rejection.

Applicants' independent claim 1 is allowable over *Fjelstad* as discussed above. *Sharma* still fails to disclose or suggest a wiring connected to a chip through a connection hole formed in a single-layer insulation film. Therefore, *Fjelstad* in view of *Sharma* still fails to disclose or suggest Applicants' claim 1.

Claims 5-6 depend directly or indirectly from claim 1 and are therefore allowable for at least the same reasons that claim 1 is allowable.

Applicants respectfully submit the rejection has been overcome and request that it be withdrawn.

E.) Rejection of claims 15-16 under 35 U.S.C. §103(a) as being unpatentable over *Fillion et al.* in view of *Sharma*:

Claims 15-16 have been cancelled.

Applicants respectfully submit that the rejection has been overcome and request that it be withdrawn.

F.) Rejection of claim 11 under 35 U.S.C. §103(a) as being unpatentable over *Eichelberger* in view of *Sudo et al.*:

Applicants respectfully disagree with the rejection.

Applicants' independent claim 7 is allowable over *Eichelberger* as discussed above. *Sudo et al.* still fails to disclose or suggest a single-layer insulation layer that encrusts a top surface and at least a portion of side surfaces of a plurality of chips. Therefore, *Eichelberger* in view of *Sudo et al.*still fails to disclose or suggest Applicants' claim 7.

Claim 11 depends directly or indirectly from claim 7 and is therefore allowable for at least the same reasons that claim 7 is allowable.

Applicants respectfully submit the rejection has been overcome and request that it be withdrawn.

G.) Rejection of claim 12 under 35 U.S.C. §103(a) as being unpatentable over *Eichelberger* in view of *Sharma*:

Applicants respectfully disagree with the rejection.

Applicants' independent claim 7 is allowable over *Eichelberger* as discussed above. *Sharma* still fails to disclose or suggest a single-layer insulation layer that encrusts a top surface and at least a portion of side surfaces of a plurality of chips. Therefore, *Eichelberger* in view of *Sharma* still fails to disclose or suggest Applicants' claim 7.

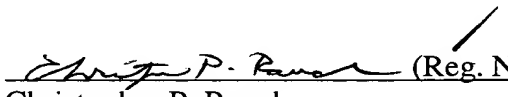
Claim 12 depends directly or indirectly from claim 7 and is therefore allowable for at least the same reasons that claim 7 is allowable.

Applicants respectfully submit the rejection has been overcome and request that it be withdrawn.

CONCLUSION

In view of the foregoing, it is submitted that claims 1-12 are patentable. It is therefore submitted that the application is in condition for allowance. Notice to that effect is respectfully requested.

Respectfully submitted,



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Christopher P. Rauch
SONNENSCHEIN, NATH & ROSENTHAL
P.O. Box #061080
Wacker Drive Station - Sears Tower
Chicago, IL 60606-1080
Telephone 312/876-2606
Customer #26263
Attorneys for Applicant(s)

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Please amend claims 1 and 7 as follows:

1. (Twice Amended) A semiconductor device, comprising:

a plurality of semiconductor chips mounted on an outer surface of a substrate;

[an] a single-layer insulation film provided on said substrate, wherein a top surface and side surfaces of said plurality of semiconductor chips are encrusted in said insulation film; and

wiring provided on said insulation film, wherein said wiring is connected to said plurality of semiconductor chips through a connection hole formed on said insulation film.

7. (Twice Amended) A semiconductor device, comprising:

a plurality of semiconductor chips;

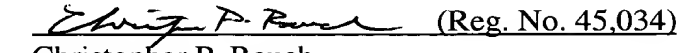
[an] a single-layer insulation layer supporting said plurality of semiconductor chips, wherein a top surface and at least a portion of side surfaces of said plurality of semiconductor chips are encrusted in said insulation layer and a surface opposite said top surface of said plurality of semiconductor chips is exposed; and

wiring provided on said insulation layer, wherein said wiring is connected to each semiconductor chip of said plurality of semiconductor chips through a connection hole formed on said insulation layer.

Please cancel claims 13-16.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited as First Class Mail in an envelope addressed to Asst. Commissioner for Patents, Washington, D.C. 20231 on February 4, 2003.

 (Reg. No. 45,034)

Christopher P. Rauch